Supervisory Control of Microgrids in Grid-Connected and Islanding Mode – Investigations Using a Real-Time Digital Simulation Platform

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***Abstract*—A robust grid structure, which makes use of distributed renewable energy generation, should consists of grid sections, which are able to seamlessly switch between grid-connected mode and islanding mode of operation. This way, failures in the upper level part of the grid can be mitigated. This contribution discusses local and supervisory control strategies, and requirements for microgrids. A robust hierarchical control structure that allows smooth transitions of the microgrid between the grid-connected and islanded mode is proposed. The proposed local controllers for the distributed energy resources are robust against disturbances, decentralized and show a reliable reference-tracking capability, which is important since transitions between operation modes involves disturbances. The local controllers represent the primary level of the proposed hierarchical control structure. To operate a microgrid in islanded mode, a centralized supervisory control structure is presented that is composed of a simple Decentralized Energy Resources (DER) coordination logic, the aforementioned local controllers, a voltage controller, and an open-loop frequency controller. To perform studies on the proposed control structures, the simulation tool PSCAD/EMTDC was used to evaluate the controller performance. Verification in a real-time digital simulator confirms the findings. The proposed control strategies appear to be robust which suggests their applicability for a use in microgrid structures. (*Abstract*)**

Keywords—grid control, microgrid, islanding mode, grid-connected mode (*key words****)***

I. Introduction

Power systems are composed of different energy resources, electrical equipment and loads. The sum of all these parts determines the overall system behaviour not only under steady-state conditions but also during faults or imbalances [1].

The depth of penetration of renewable energy sources within power grids will continue to increase which is accompanied by a changing system behaviour [2]. For a better controllability of those changing power systems topologies, microgrids are a useful tool. If the control structure for microgrids is well chosen and implemented, they can provide additional functions like auxiliary services, reduced losses, improved reliability, peak load reduction, reduced costs and a reduction of emissions [3-6].

The control structure needs to meet certain criteria to handle disturbances and faults such as:

- Reliably recognize fault conditions in the host-system to initialize the islanding process
- Reliably recognize recovery of the host-system to initialize the reconnection process
- Detection of islanding and grid reconnecting conditions within a short time.
- Transients are minimized to avoid damage to electrical equipment or system instabilities.
- Power system reaches steady-state after transition within a short time
- In Islanded Mode, power to the loads is provided while keeping the microgrid system frequency and voltage constant.

To achieve those criteria, a fitting control scheme is developed. Therefore, a realistic microgrid study system with its associated supervisory and local controls is developed and analyzed in PSCAD/EMTDC. To validate the findings, a simplified version of the system was remodelled in a real-time digital simulator.

II. Study System

The AC-microgrid consists of symmetrical, three-phase, radial distribution feeders with a nominal voltage of 13.8 kV. The study system includes three feeders, three DER units and three loads. At the point of common coupling (PCC) it is connected to the utility grid through a 69.0 kV line. The configuration and parameters are adopted from a benchmark system and is showed in Figure 1 [7].

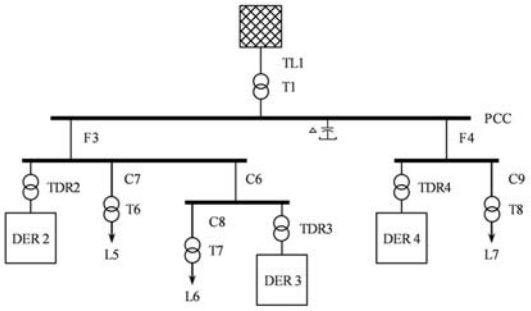

Figure 1. Study System

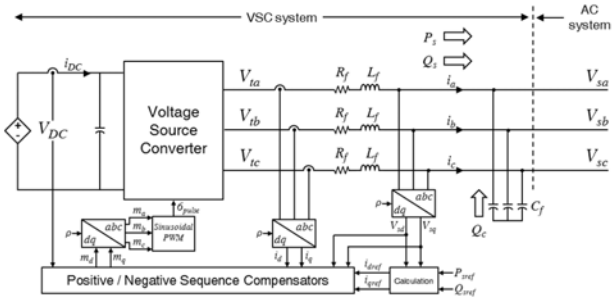

Figure 2. Schema of the current-controlled VSC

The utility grid is modeled by a three-phase, ideal voltage source with a short-circuit apparent power of 100 MVA, an X/R ratio of 22.2 and a nominal voltage of 69.0 kV. At the 15 MVA transformer T1 the voltage is stepped down from 69.0 kV to 13.8 kV and is in delta-star-to-ground configuration.

Additionally, there is a 2 MVAr fixed shunt capacity bank in delta configuration at the PCC which is smoothens the transition when switching between grid-connected and islanded mode.

The loads L5, L6 and L7, represented by series L and R branches, are three phase balanced loads.

The three DER units are dispatchable and have a rated voltage of 0.6 kV. The power ratings are 3.0 MVA for DER2 and DER3, and 0.5 MVA for DER4.

Each DER unit includes a two-level DC/AC-voltage-sourced converter (VSC) with sinusoidal pulse-width modulation (SPWM). The DER DC-side is rated at 1.2 kV and modeled by two voltages sources which are in series.

L_f, C_f and R_f form the low-pass filter at the VSC terminal, which is necessary because the VSC terminal voltages are modulated waveforms. If not present, the voltages $V_{s,abc}$ would have voltage notches disturbing the feedback signals V_{sd} and V_{sq} as well as the load voltage. The LC filter is tuned to the dominant pulse-width modulation side-band harmonic and VSC current harmonics, which flow through the filter, will cause no disturbance in the upstream grid. R represents switching losses [8].

The real and reactive power is controlled by the line currents given as dq-frame parameters i_d and i_q. Based on the angle ρ, given by the phase locked loop, the 3-phase signals are converted into dq-frame signals and then processed by the corresponding compensators to give the control signals. Before the signals are fed to the VSC, they are transformed back to the abc-frame, namely m_{abc}. Afterwards, the signals are forwarded to the sinusoidal pulse-width generator, which creates six gating pulses for the VSC switches to output the required active or reactive power. An overview of the VSC is displayed in Figure 2.

III. Control Strategy

In the chosen control strategy, there are two levels of controllers, that are (i) decentralized primary controllers which are located at each DER unit and (ii) a centralized supervisory controller which is located within the microgrid close to the PCC.

A. Primary Controller Strategy

The proposed control strategy is to ensure that the control objectives are met in case of pre-defined islanding as well as in case of a fault occurring on the utility grid. Since the DER units are modelled as PV arrays the microgrid will have fast dynamic characteristics. Therefore, the control needs to react in the order of cycles to meet the system requirements.

Two reasons for the islanding were investigated: (i) due to pre-defined islanding for maintenance purposes at the utility grid side or (ii) unintentional islanding caused by a fault in the AC-host system.

In grid-connected mode, an active/reactive power controller is used which follows given set points for the output of active/reactive power to the grid. This controller is referred to as PQ-controller. The used topology is called current-mode control and protects the VSC from overcurrent, since the line-current is regulated through the VSC AC-side voltages. Additionally, this control topology has a good dynamic performance, a high control precision and a certain robustness related to the variation of the VSC- and AC-system parameters. The only demerit is, that a phase-locked loop is needed in addition [9].

In islanded mode, a voltage and frequency controller is activated to respond to the condition of islanding. In response to the missing connection to the main grid, the voltage and frequency at the PCC is expected to drop. The now activated controller will control and adjust the measured 3-phase voltages to their nominal voltages, as well as provides a reference frequency for the microgrid. This controller is called controlled-frequency VSC which provides overcurrent and overload protection. This controller is referred to as VF-controller.

B. Supervisory Controller Strategy

The centralized microgrid supervisory controller coordinates the processes within the microgrid and acts as a tertiary controller above the aforementioned local controllers within the hierarchical controller structure [10].

The first task of the supervisory controller is the islanding detection. Voltage and frequency of the utility grid are constantly monitored. However, a disturbance in the AC system, if planned or unintentional, causes considerable deviations in the monitored voltages V_{gabc}, V_{sabc} as well as in the frequency. After a reasonable small detection delay the voltage deviation is recognized by the supervisory control and sends a signal to the main circuit breaker, which couples the microgrid with the utility grid. The breaker of each phase will open only at the next zero-crossing which causes another time delay. After the monitored breaker current of each phase becomes zero, the VSC systems gets the signal to switch from the grid-imposed PQ-mode to the controlled-frequency VF-mode. In this case, the master DER unit starts to regulate the load voltages about their correspondent nominal values and provides a reference frequency.

The second task of the supervisory controller is the detection of the restored utility grid. After the AC-host grid recovers to normal condition, the voltage V_{gabc} return to their nominal voltages as well as the utility grid frequency. Only if V_{gq} is within a small range of its nominal voltage, which is zero, and a grid frequency close to 60 Hz, the controller considers the AC system to be restored. As a result, the VCO switches from signal w_0, provided by the VF-controller, to the grid frequency based on V_{sq}. Following, the supervisory control gives a signal to the main circuit breaker for reconnection and the control mode switches from VF- to PQ-mode with a grid-imposed frequency.

The third task is the coordination of DER units. The controller determines one DER to be the master unit. This unit, in the case of islanding, switches to VF-mode to control the voltage at the PCC, and gives a reference frequency, while the other DER units will remain to operate in the PQ-mode.

IV. Controller Design And Implementation

The design and implementation of the different controllers are based on the guidelines provided in [8].

A. Primary Controller Implementation

1) PQ-controller:

The VSC model in dq-frame can be defined by

$$V_{td}(t) = \frac{V_{DC}}{2} m_d(t), \tag{1}$$

$$V_{tq}(t) = \frac{V_{DC}}{2} m_q(t). \tag{2}$$

The control of P and Q in dq-frame is written as

$$L\frac{di_d}{dt} = L\omega_0 i_q - (R + r_{on})i_d + V_{td} - V_{sd}, \tag{3}$$

$$L\frac{di_q}{dt} = -L\omega_0 i_d - (R + r_{on})i_q + V_{tq} - V_{sq} \tag{4}$$

with V_{td} an V_{tq} being control inputs, i_d and i_q being state variables and V_{sd} and V_{sq} being disturbance inputs. Since the dynamics of the two state variables i_d and i_q are coupled with each other through the term $L\omega_0$, they can be decoupled by the following equations

$$m_d = \frac{2}{V_{DC}}(u_d - L\omega_0 i_q + V_{sd}), \tag{5}$$

$$m_q = \frac{2}{V_{DC}}(u_q + L\omega_0 i_q + V_{sd}) \tag{6}$$

with u_d and u_q being new control inputs. As a result, (3) and (4) can be rewritten

$$L\frac{di_d}{dt} = -(R + r_{on})i_d + u_d, \tag{7}$$

$$L\frac{di_q}{dt} = -(R + r_{on})i_q + u_q \tag{8}$$

The equations above now resemble two linear, first-order, decoupled systems. Based on the shown equations in this section, the d- and q-axis current controller can be implemented [8]. The control block diagram for the controller is displayed in Figure 3.

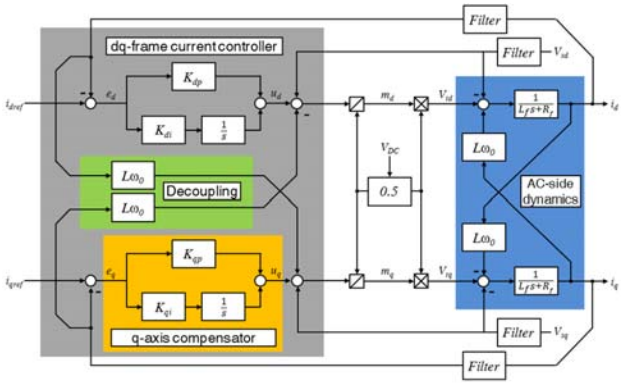

Figure 3. Current-controlled VSC control block diagram. Based on [2].

The signals u_d and u_q can control i_d and i_q. The input of the d-axis compensator $k_d(s)$ is $e_d = i_{dref} - i_d$ and gives u_d at the output. Signal u_d together with the feedback and feed-forward signals leads to m_d. The VSC amplifies this signal to gain V_{td}, which in turn controls i_d.

Since the compensator tracks DC reference commands, it is adequate to use a simple PI controller here, which has the form

$$k_d(s) = \frac{k_p s + k_i}{s}, \qquad k_d$$

As proposed in [8], the ideal way to tune the compensator is, to select k_p and k_i based on

$$k_p = \frac{L_f}{\tau_i}, \tag{10}$$

$$k_i = \frac{R_f}{\tau_i}, \tag{11}$$

whereas τ_i is chosen to 1.25 ms.

2) VF-Controller:

Similar to the PQ-controller where ω can be imposed via PLL, the controlled-frequency VSC regulates V_{sabc}, which can be defined in dq-frame as

$$\hat{V}_s = \sqrt{V_{sd}^2 + V_{sq}^2}.$$

The capacitator C_f which has to be taken into account. The load voltage dynamics in dq-frame can be described as

$$C_f \frac{dV_{sd}}{dt} = C_f(\omega V_{sq}) + i_d + i_{Ld}, \tag{13}$$

$$C_f \frac{dV_{sq}}{dt} = -C_f(\omega V_{sd}) + i_d - i_{Lq}. \tag{14}$$

A feed-forward compensation, as before for the PQ-controller, is used to decouple V_{sd} and V_{sq} which enables the possibility to control V_{sd} by i_{dref} and V_{sq} by i_{qref}. This can be expressed by the following equations

$$i_{dref} = u_d - C_f(\omega V_{sq}) + i_{Ld}, \tag{15}$$

$$i_{qref} = u_d + C_f(\omega V_{sd}) + i_{Lq}. \tag{16}$$

For the VF-controller, a PI compensator is proposed with the form

$$k(s) = k\,\frac{s+z}{s}.$$

To develop this compensator, the guidelines in [7] suggest to calculate the gain k to

$$k = C_f \omega_c,$$

where ω_c is the cut-off frequency in rad/s. For calculating z the following two equations can be used:

$$\delta_m = \sin^{-1}\left(\frac{1-\tau_i z}{1+\tau_i z}\right), \tag{19}$$

$$\omega_c = \sqrt{z\tau_i^{-1}} \tag{20}$$

The selected phase margin δ_m is typically chosen between 30° and 75° [8]. The VF-controller is shown in Figure 4.

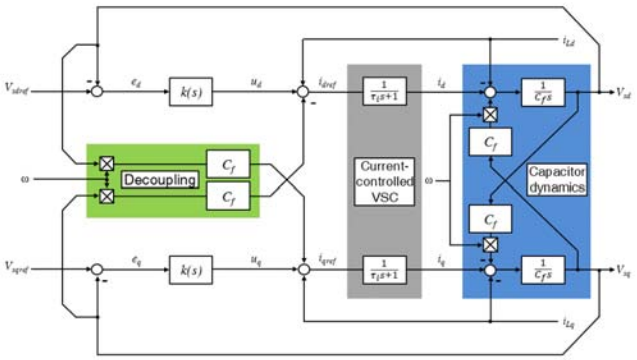

Figure 4. Controlled-frequency VSC control block diagram. Based on [2].

B. Supervisory Controller Implementation

1) Grid Monitoring:

To execute its tasks, the supervisory control needs to monitor the grid, especially the grid voltages V_{gabc} and the grid frequency $f_{PLL,UG}$. Thus, a phase-locked loop is implemented with respect to [8] and shown in Figure 5.

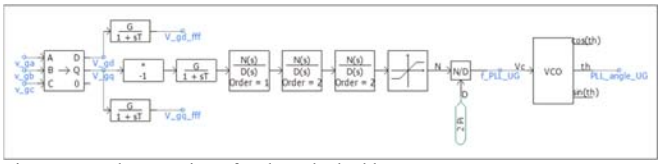

Figure 5. Implementation of a phase-locked loop

2) Islanding Process:

At the PCC, the voltages V_{gabc} are monitored and transformed to their dq-frame quantities, that are V_{gd} and V_{gq}. As a result, V_{gpeak} can be calculated as follows

$$\hat{V}_{gpeak} = \sqrt{V_{gd}^2 + V_{gq}^2}. \tag{21}$$

Afterwards, this signal is passed through a low-pass filter and a range comparator. The output of the comparator provides

$$\begin{aligned} Output &= 0 \quad if \quad \hat{V}_{gpeak} > 12.6\,kV \\ Output &= 1 \quad if \quad 10.0\,kV \le \hat{V}_{gpeak} \le 12.6\,kV \\ Output &= 0 \quad if \quad \hat{V}_{gpeak} < 10.0\,kV \end{aligned} \tag{22}$$

as logic signal, which is fed to the SET-input of a RS latch. Since the output of the comparator is 1 when V_{gpeak} is in the desired range, the SET-input is inverted.

If S = 1, then Q = 1 which is signal name is $CB_{UG,Main}$. The main circuit breaker will get a logic 1 which will initialize the opening of the switch. The switch only opens after each phases zero crossing and therefore, no current chopping is allowed. The switch internal outputs are activated in order to monitor the 3 breaker current signals, namely $i_{CB,Main,a}$, $i_{CB,Main,b}$ and $i_{CB,Main,c}$. Each signal is send to a range comparator that gives

$$\begin{aligned} Output &= 0 \quad if \quad i_{CB\_Main\_abc} > 0.1\,A \\ Output &= 1 \quad if \quad -0.1\,A \le i_{CB\_Main\_abc} \le \\ Output &= 0 \quad if \quad i_{CB\_Main\_abc} < -0.1\,A \end{aligned} \tag{23}$$

To ensure that not every zero-crossing is forwarded as logic 1 to the next block but only those for which the current afterwards stays zero, a binary-ON-delay-block is used at the output of each range comparator.

The 3 current signals $i_{CB\_Main\_abc}$ are then fed into a logic AND-block, which ensures that the output becomes only then a logic 1, when all 3 inputs become 1. It becomes 0 as soon as one of the inputs is 0. The output of this AND-block is the signal $CB_{UG\_MAIN\_ZC}$.

The two signals $CB_{UG\_MAIN\_ZC}$ and CB_{UG_Main} are fed into another AND-block, which output is finally the signal VFSignal. This signal triggers the master DER units to switch from PQ- to VF-mode.

The developed and implemented control block diagram for islanding detection is displayed in Figure 5.

3) Reconnection Process:

To enable the supervisory controller to detect whether the AC-host system has returned to normal conditions, the signal V_{gq} first is divided by its nominal value, which can be calculated to

$$\hat{V}_{gq,n,L2G} = V_{gn}\sqrt{\frac{2}{3}} = 13.8\ kV * \sqrt{\frac{2}{3}} = 11.268\ kV_{qpeak} \quad (24)$$

and afterwards fed to a low-pass filter and range detector. The filter smoothens the signal and the output of the comparator provides

$$\begin{aligned} Output &= 0 \quad if \quad V_{gq} > 0.03\ kV \\ Output &= 1 \quad if \quad -0.03\ kV \leq i_{CB\_Main\_abc} \leq \\ Output &= 0 \quad if \quad V_{gq} < -0.03\ kV \end{aligned} \quad (25)$$

Therefore, if V_{gq} is in the desired range ± 3% of 0 kV. This logic signal is fed to an AND-block with 2 inputs.

Next, the signal f_{PLL_UG} which is the monitored AC-host system frequency is fed to low-pass filter and a range comparator with

$$\begin{aligned} Output &= 0 \quad if \quad f_{PLL\_UG} > 60.10\ Hz \\ Output &= 1 \quad if \quad 50.90\ Hz \leq f_{PLL_{UG}} \leq \\ Output &= 0 \quad if \quad f_{PLL\_UG} < 50.90\ Hz \end{aligned} \quad (26)$$

This is the second input of the AND-block. Only if both signals V_{gq} and $f_{PLL,UG}$ are logic 1, the output of the AND-block becomes 1 and is referred to as signal L_{VqANDf}. This signal is fed to the RESET-input of the RS latch described in the section before. Resetting the RS latch will set signal $CB_{UG,Main}$ to zero leading to a closure of the circuit breaker in order to reconnect the microgrid to the host grid as displayed in Figure 6.

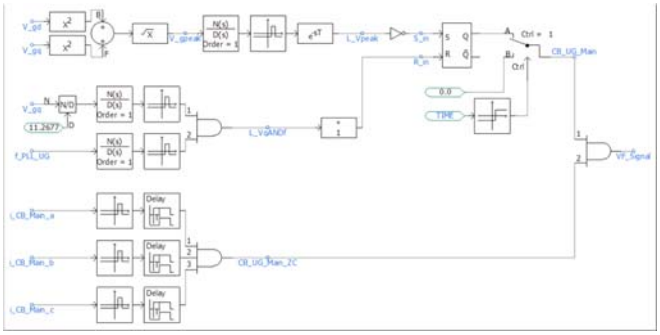

Figure 6. Islanding detection, and grid reconnection control block diagram.

V. Results

Three different test cases are conducted: (i) intentional island, (ii) 3-phase to ground fault and (iii) 1-phase to ground fault. The simulations were performed off-line first and then validated on a real-time digital simulator.

A. Intentional Islanding

1) Off-line Simulation

The DER units adjust their real and reactive power output according to the power consumption within the microgrid as a result of the existing loads. After the DERs have adopted their power generation, the circuit breakers both from the utility grid and at the PCC will open to initiate the islanding mode. The pre-selected master DER unit – which is in VF-mode – will provide the islanded microgrid with a reference frequency and adapt P and Q to the load voltages if necessary to stabilize the voltage within the microgrid to its nominal value.

At t = 0.52 s the utility side circuit breaker opens and due to an artificial build-in detection delay within the supervisory control, the opening of the utility grid breaker is detected at t = 0.54 s only. The supervisory control operated breaker opens with a delay, because it can open the breaker of each phase only at the corresponding zero-crossing of the currents.

At t = 0.545 s the microgrid is decoupled from the utility grid. The pre-selected master DER unit, in this case the DER_2, now dictates the reference frequency of 60 Hz. The transition from grid-connected mode to islanded mode is uneventful and only very small voltage deviations were apparent at the PCC. The same is true for the transition from islanded to grid-connected mode at t = 0.650 s.

It can be observed that there are deviations between the desired P and Q set point right before and shortly after islanding. This is partly the result of the detection delay of the supervisory control. Furthermore, after DER_2 is in VF-mode, it takes some time until the controller has adapted its real and reactive power output, such that power generation and power consumption are balanced and, therefore, the microgrid voltage is stable.

Moreover, although the DER units adjusted their real and reactive power output before islanding, it is apparent that a surplus of reactive power is existing. This is caused by the capacitor bank which is bound at the PCC. The additional reactive power in this case is absorbed by the DER_2.

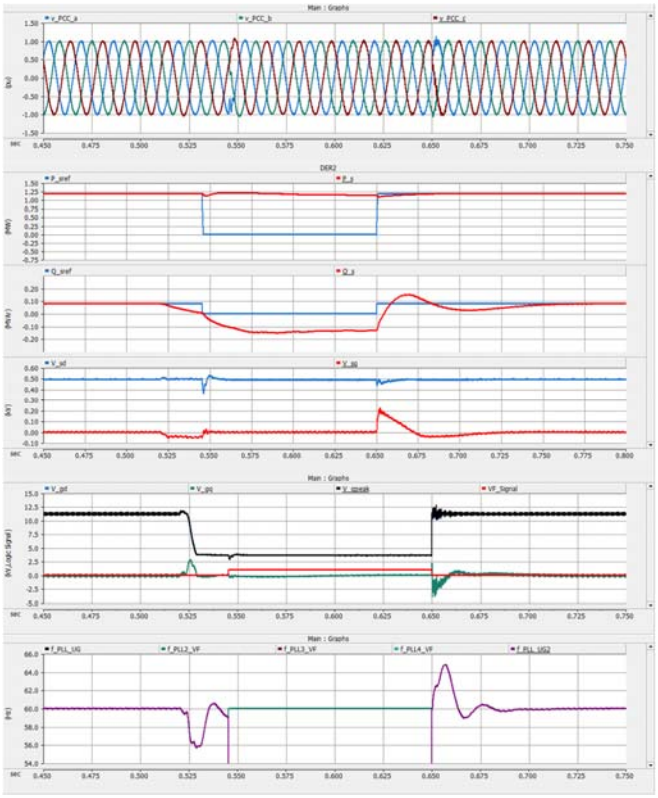

Figure 7. Intentional Island - Off-line simulation

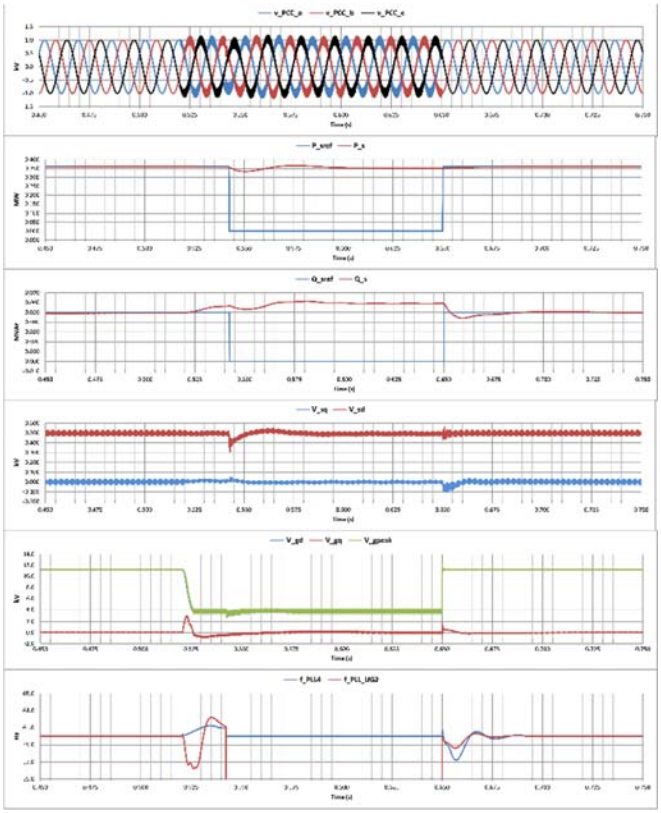

Figure 8. Intentional Island - Real-time simulation

Figure 6 displays which entity provides the reference frequency. Until t = 0.545 s the frequency is provided by the utility grid. Afterwards DER_2 is in charge and dictates the frequency to be 60 Hz for the microgrid. As the microgrid reconnects, the main grid again controls the frequency. At the time point of reconnection, the frequency experiences a disturbance and reaches steady state at t = 0.690 s only.

2) Real-time Simulation

The real and reactive power output is adjusted before islanding, so that while transition to islanded mode power deviation is small. The voltages at PCC show no major deviations, as displayed in Figure 7. However, the signal is afflicted with noise, because no capacitor bank was modeled for the test in RTDS. The current over the circuit breaker is almost zero, since DER_4 provides the necessary power to its load. The breaker opens at t = 0.535 s. When reconnecting at t = 0.65 s, a current deviation over the breaker is apparent.

The signals V_{sd} and V_{sq} show that during both transitions no large voltage deviation occurs and, while in islanded mode, the microgrid – controlled by DER_4 – is in steady state. The latter one is achieved by the supervisory control in keeping Vsq close to zero. Examining the monitored signals of the supervisory control, it is observable that the transitions between modes causes small deviations in the frequency.

B. *Fault: 3-phase to ground*

1) Off-line Simulation

In this test case, a three-phase to ground fault at the PCC is investigated. The AC-microgrid will experience an unintentional islanding and the real and reactive power outputs of the DER units will not be adapted to their loads' needs before transitioning into the islanded mode. The real power outputs for each DER unit is at maximum whereas the reactive power output is at zero. Since the fault is a three-phase fault, it is balanced and, hence, a less severe test case. The fault is applied at t = 0.5 s when the system is in steady state and power is provided by the DERs. The duration of the fault is 0.15 s. An artificial detection delay of 0.02 s is applied to the supervisory control to receive a more realistic system response.

Examining the voltages of the PCC, it is apparent that the fault causes the voltages $v_{PCC,abc}$ to drop down to 0.675 pu. After the detection delay of the supervisory control has passed, the control recognizes that the pre-conditions for islanding are met and initiates the process. The circuit breaker $CB_{UG,Main}$ receives the order to open at t = 0.52 s, but has to wait for each phase to reach its next zero crossing. The circuit breaker opens at t = 0.525 s, and the preselected master DER unit switches from PQ- to VF-mode and provides the now islanded microgrid with reference voltage and frequency. The observed voltage disturbances caused at the PCC before islanding are shown in Figure 9.

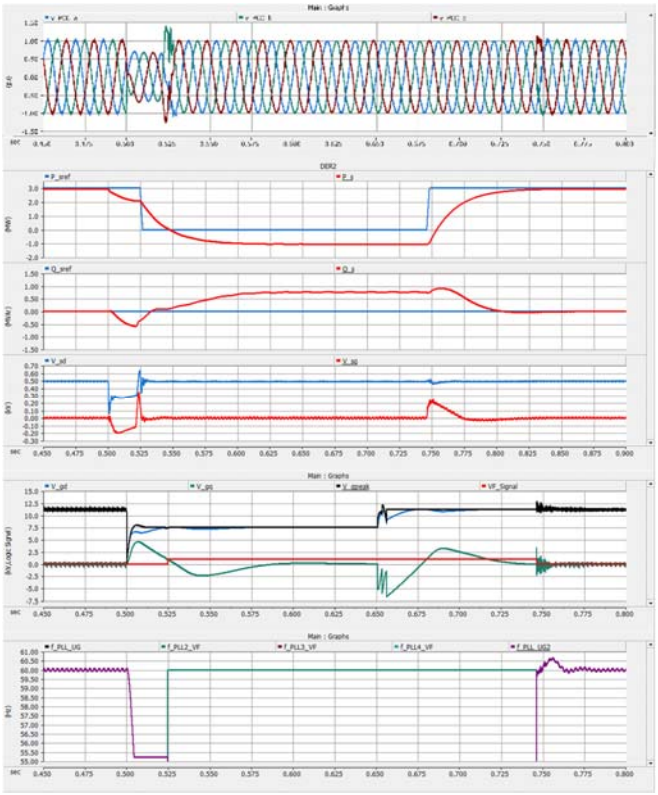

Figure 9. Fault: 3-phase to ground - Off-line simulation

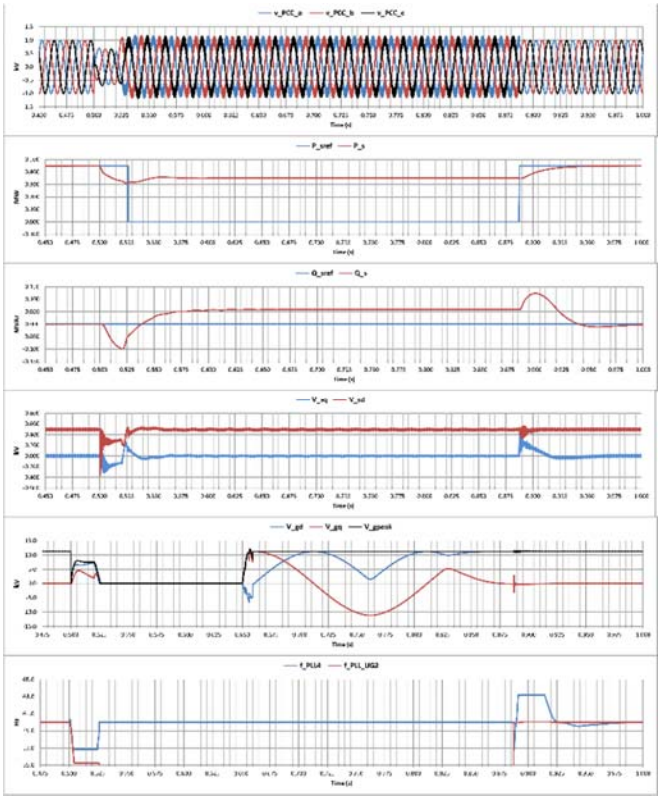

Figure 10. Fault: 3-phase to ground - Real-time simulation

DER_2 switches to VF-mode to provide voltage and frequency for the microgrid. It monitors the load voltages, V_{sd} and V_{sq}, and adapts the real and reactive power. The simulation exhibits that DER_2 must supply additional reactive power whereas the generated power within the mircrogrid is too high. Therefore, it absorbs real power which can be stored in an energy storage system.

Examination of the supervisory control monitored signals show that because of the fault the frequency at PCC as well as the monitored voltages, which are transformed to V_{gd} and V_{gq}, decrease abruptly. Start and end of the fault can be easily identified via signal $V_{g,peak}$, since it is reduced in that time .

As mentioned before, at t = 0.525 s, the breaker opens and the microgrid switches into islanded mode. Before the fault, until t = 0.5 s, the frequency given by the utility grid, namely $f_{PLL,UG2}$, is the reference frequency and remains responsible although at its lower threshold until the supervisory control delay is over and can decouple the microgrid while switching to VF-mode. At this time, the pre-selected DER unit is in charge to provide the reference frequency, namely $f_{PLL2,\,VF}$. The fault ends at t = 0.65 s and the grid voltages return to pre-disturbance conditions. However, the supervisory control allows reconnection to the main grid only when the grid frequency (i) returns to 60 Hz and (ii) reaches a steady state which is when V_{gq} remains zero. Both conditions are met at t = 0.746 s, the supervisory control initiates reconnection and DER_2 returns from VF- to PQ-mode. The time in which the microgrid is islanded can be identified by a high VF_{Signal}.

2) Real-time Simulation

A significant difference to the off-line simulation is that the system takes longer until the pre-conditions are met to reconnect with the main grid. During the detection delay, the PCC voltages are reduced to 0.64 pu and return to 1 pu after switching into VF-mode. Again, the noise at the PCC is high, although it is visible that the voltages return to their pre-disturbance magnitude. The voltage deviation seems lesser compared to the off-line simulation.

DER_4 adapts its real and reactive power output to the needs of the islanded microgrid. It reduces its real power output to support the load. The load voltage deviation, seen in signal V_{sd} and V_{sq}, appears to be similar but more severe than in the off-line simulation.

The grid signals during the transition to the islanded mode appears to be different. In the off-line simulation signal V_{gd} drops at first, then recovers to 7.5 kV. In the real-time simulation, V_{gd} also recovers at first to 7.5 kV, but then becomes zero. After the fault is removed at t = 0.65 s, it takes longer for V_{gd} and V_{gq} to reach a steady state and, therefore, until the pre-conditions are met which allow the microgrid to reconnect to the main grid. The main grid returns to steady state at t = 0.885 s. Furthermore, the reconnection is less smooth, because the frequency of the utility grid overshoots at the beginning until it reaches its upper frequency limit at f = 65 Hz. The off-line simulation overshoot is only as high as 0.5 Hz. The results are shown in Figure 10.

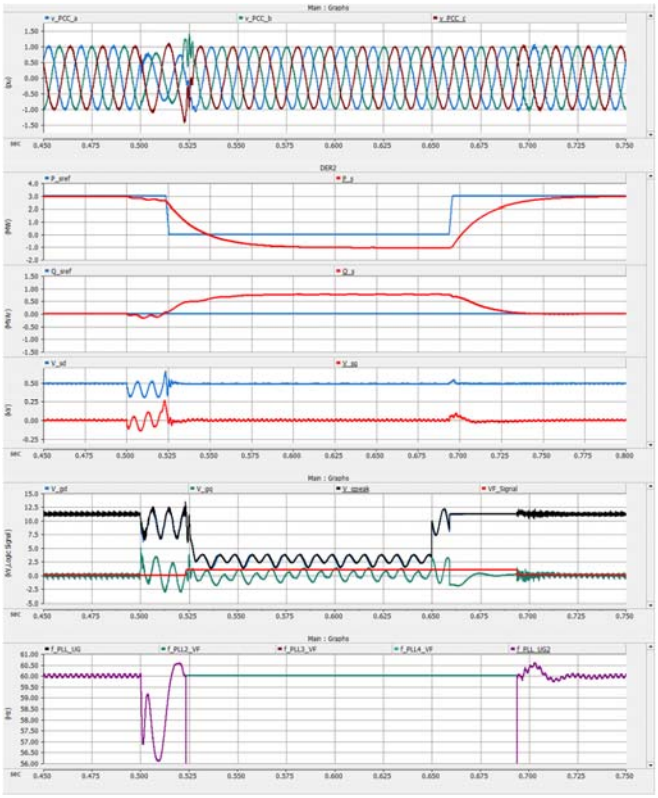

Figure 11. Fault: 1-phase to ground - Off-line simulation

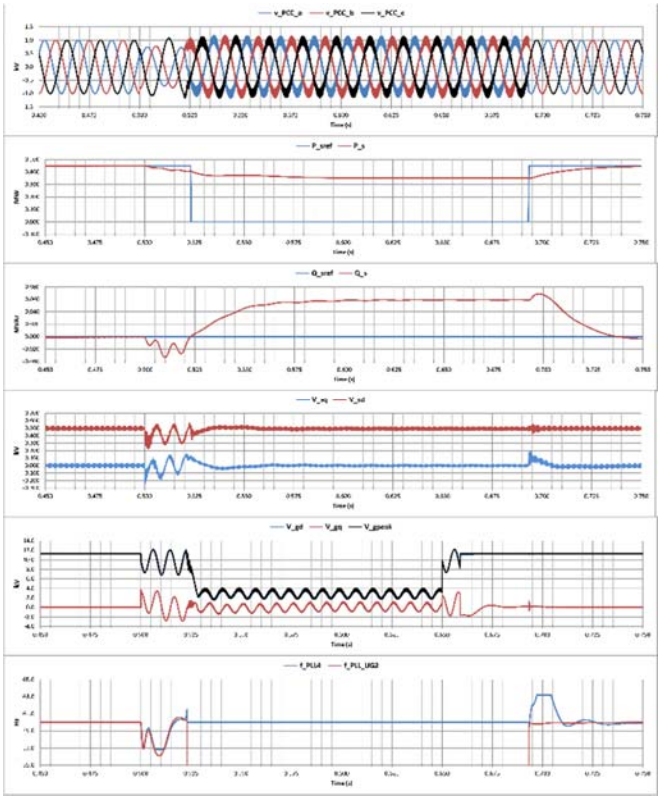

Figure 12. Fault: 1-phase to ground - Real-time simulation

C. *Fault: 3-phase to ground*

1) *Off-line simulations*

This test case examines the system response to a single-phase-to-ground fault, which is more severe than the previous case. The DER units generate real power at their maximum level while no reactive power is provided. The fault is applied at t = 0.5 s while the system is in steady state, and ends after 0.15 s. The fault is detected by the supervisory control after 0.02 s at t = 0.52 s.

Investigating the PCC voltages indicates that, after the fault occurs and before the supervisory control recognizes it, the voltage amplitudes of the different phases vary from each other and over time between 0.7 pu and 1.43 pu. At t = 0.524 s the switch of the main circuit breaker opens and the microgrid operates in islanded mode. The very first moments after the switching causes high voltage deviations of up to 1.4 pu at the PCC which last less than one cycle. After the fault is removed and the pre-conditions for reconnecting to the utility grid are met, the voltage deviations are neglectable. The system behaviour is shown in Figure 11.

Compared to the previous case, strong oscillations occur between the beginning of the fault conditions and the switching. As soon as the microgrid is in islanded mode, the oscillations stop.

Since DER_2 is the pre-selected master unit, it changes from PQ- to VF-mode. It provides the reference frequency and regulates the load voltages V_{sd} and V_{sq}. Since the provided power is higher than what is needed by the loads, DER_2 absorbs the surplus of power.

The utility grid signals display a different pattern compared to the previous, balanced fault test case. Instead of dropping to a certain value, both grid voltages and frequency keep oscillating. After the microgrid is disconnected, the oscillations of the grid voltages and the frequency become smaller, since the fault is not fed by the DER units anymore. The fault is removed at t = 0.65 s. However, the grid frequency does not stabilize before t = 0.694 s. The microgrid itself is in steady state after 0.1 s that is at t = 0.625 s.

2) *Real-time simulation*

Voltage deviations are observed but not as distinctive as with the off-line simulation. Those diverging results are shown in Figure 12.

In the grid-connected mode, DER_4 only outputs real power, whereas in transition no big fluctuations are apparent. The reactive power is set to zero before islanding and will be increased to match the loads consumption. Signals V_{sd} and V_{sq} show an oscillating behaviour, similar to the off-line simulation. The microgrid reaches its steady state within 0.05 s and the reconnection is smooth.

The grid signals show a similar behaviour as in the off-line simulations. The system values keep oscillating until the fault ends and return within short time to steady state conditions.

VI. Conclusion

The proposed control strategy is robust against a variety of disturbances, which is shown in the three different test cases for both off-line and real-time simulations.

The local controllers of the DER units are capable to handle both symmetrical and unsymmetrical fault conditions. Furthermore, the local controllers can dynamically adept the real and reactive power while they are in the voltage- and frequency control mode to supply the loads adequately and maintain the microgrid stability.

The supervisory control showed a reliable fault detection capability since all tested fault scenarios where successfully recognized and a transition to the islanded mode was initiated. Additionally, the AC-host system status was successfully tracked and the supervisory control initiated the reconnection only if the AC-host system recovered to pre-disturbance conditions.

A simplified study system consisting of the AC-host system, DER unit 4 and load 7 was re-modelled in RSCAD to examine the system behavior in a real-time digital simulator. The findings of the PSCAD/EMTDC simulations could be verified.

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